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APPLICATIONS FOR LOW LEAKAGE DIODES

In circuit designs for sensor signal conditioning, the design engineer must protect the input section from over-current and over-voltage conditions. Op-amps, ADC analog inputs, analog multiplexers, and [RS485] line receivers represent classes of devices that need protection. Often, the manufacturers of such devices specify the acceptable input range for voltage, or, in the case of an overvoltage condition, the allowable input current above which semiconductor or bonding wires may be damaged.

Note that an overcurrent condition may not cause immediate failure of the device, but instead may degrade the input device (increase offset voltage, increase bias current, increase noise, etc.). A typical input circuit voltage clamp using general purpose diodes such as 1N4148 and an op-amp such as the OPA604 is shown in Figure 1. Note that some details have been omitted for clarity, such as power supply bypass capacitors, frequency compensation components, and input bias current resistors.

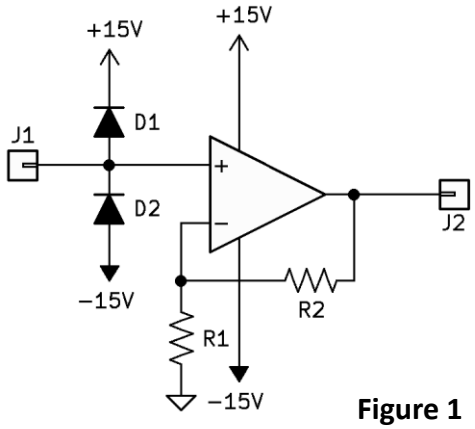

Figure 1

In this circuit, the diodes D1 and D2 connect to reference voltages that are the same as the op-amp's supply voltages. If a voltage greater than the supply rails plus the voltage drop across one silicon diode (typically 0.6V) is applied to J1 the diodes D1 and D2 limit the voltage from appearing at the op-amp's positive input. In real world applications, the over-voltage might be due to electro-static discharge; high-voltage arcing (welding equipment, X-ray generators); system power connections making contact with the J1; or, in the case of bio-medical monitoring devices, high-voltage pulses from cardiopulmonary resuscitation devices. See Reference 1 for a discussion of discharges of static electricity from someone touching the circuitry. Since we don't know the characteristics of this over-voltage source (low or high impedance; limited or virtually unlimited current), we would add extra resistance between the diodes and J1. For additional protection, we might also add extra resistance between the diodes and the op-amp. This improved version with R3 and R4 is shown in Figure 2.

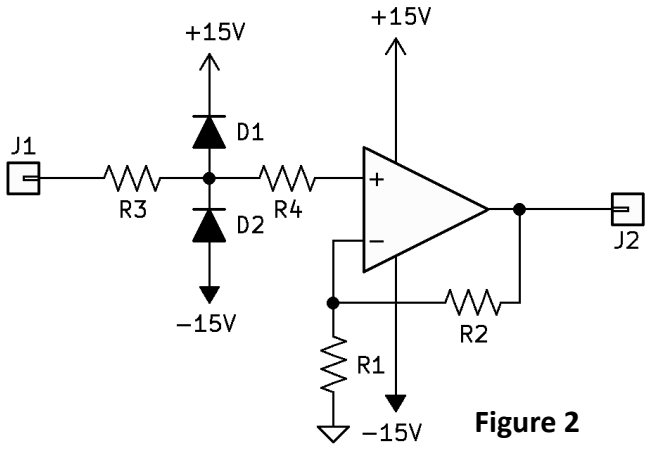

Figure 2

A variation on the previous circuit is the transimpedance (current-to-voltage) amplifier, shown in Figure 3. Note that at first glance, this looks like a voltage amplifier with R1 as the feedback resistor and R3 as the input resistor. In practice, R1 is very large compared to R3 and the voltage drop across R3 is trivial considering the extremely low signal currents being measured.

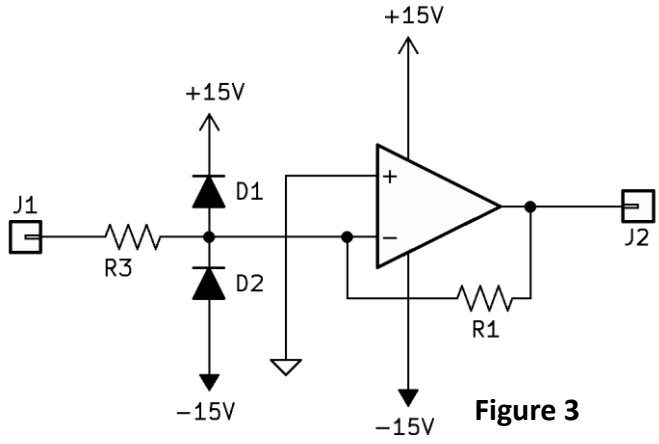

Figure 3

For many applications, this configuration would be good enough. But if the sensor output is very low (in the microvolts or pico- to femto-amps order of magnitude), measurement errors will occur.

For the circuit in Figure 2, the leakage current through the diodes creates a voltage at the junction of R3, R4, D1, and D2 that can swamp out the voltage being measured. For the circuit in Figure 3, the leakage current through the diodes may well be on the same order of magnitude as the current being measured. Examples of such current output sensors include photodiodes, photomultiplier tubes, Geiger-Müller tubes, piezo transducer accelerometers, and electrometers.

One way to reduce the diode leakage current is to use lower reference voltages at the top of D1 and the bottom of D2. For example, with ±5V instead of ±15V, the leakage current is lower. Keep in mind that the permissible signal voltage swing at the input is limited and the junction capacitance of the diodes will be higher in this scenario. More on junction capacitance induced problems in a bit.

A slight variation in lowering the reference voltage consists of a method to vary the reference voltage so it tracks the input voltage. See Figure 4 for a typical circuit. This sometimes referred to a bootstrapped drive and it touches on some of the same issues for which guard traces are used on a PC board. An excellent discussion of methods to guard sensitive circuits and minimize leakage currents across the surface of the PC board is available in Reference 2.

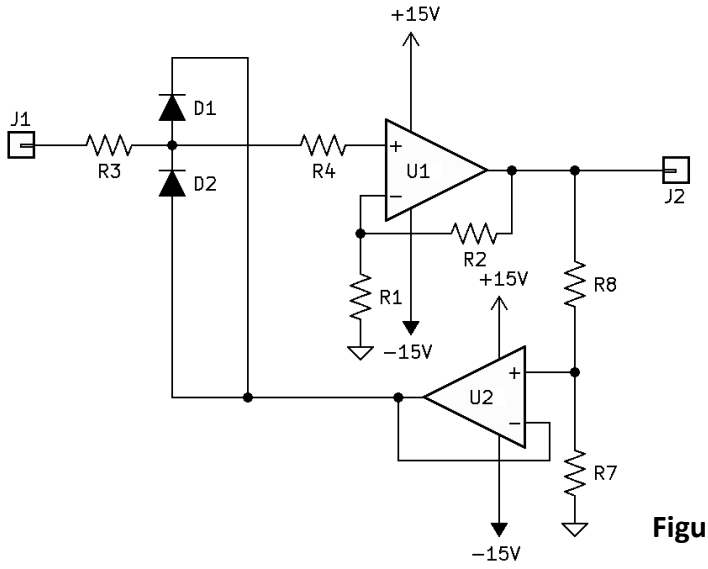

Figure 4

Note that R7 and R8 reduce the drive to U2 by an amount slightly greater than the gain of U1 (set by R1 and R2). This prevents the bootstrap circuitry from latching up or oscillating.

An additional application that has similar constraints is the sample-and-hold (S/H) circuit. The S/H is used to capture an analog signal and hold the value (voltage) steady while an analog-to-digital converter performs a conversion. See Figure 5 for a simplified version. The voltage on C1 follows the input voltage at J1, although with a slight lag based on the RC time constant. That time constant (in seconds) is the product of the sum of the resistance R3 plus the on-resistance of the analog switch (in Ohms) times the value of C1 (in Farads). At regular intervals, the Sample/Hold command is issued. As before, leakage current in diodes D1 and D2 will cause errors in the voltage measurement. Note that additional errors may be introduced due to charge injection from the analog switch.

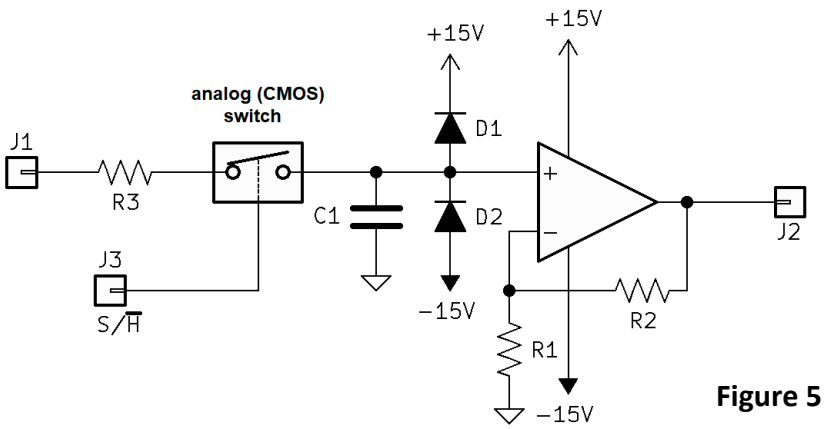

Figure 5

A variation on the S/H is the peak detector, shown in Figure 6. The voltage on C1 follows the input voltage minus the typical voltage drop across the diode (approximately 0.6V). At predetermined intervals, a RESET command is issued that returns the voltage on the capacitor to zero. Leakage in D3 will also cause measurement errors.

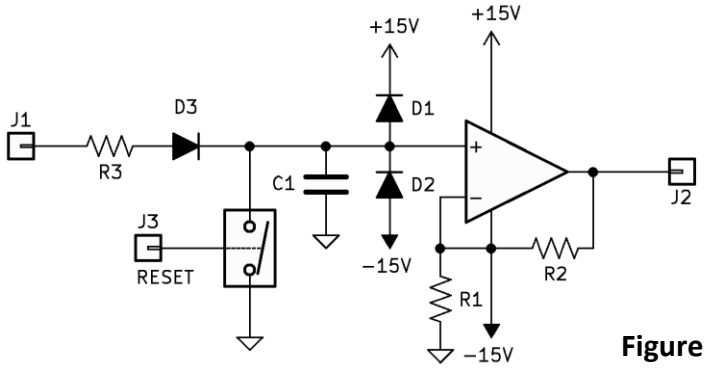

Figure 6

An additional consideration in all of the previous circuits concerns frequency response. While some of the sensors cited above are outputting signals that don't change quickly (i.e., low rate of repetition or low frequency), some may have high rep-rates or rapid slew rates. On signals with rapid slew rates, even if the rep-rate is slow, the signal's frequency spectrum is wide and the amplifier circuitry must have wide frequency response. If the clamp diodes have relatively high junction capacitance, their capacitance and the input resistor (R3, Figure 2) create a low pass filter and limits overall high frequency response. Worse yet, excessive capacitance at the transconductance op-amp's summing junction (op-amp's minus input, Figure 3) can cause excess signal overshoot (ringing) or oscillation.

An excellent solution to the problem of diode leakage is to use diodes specifically designed to exhibit ultra-low leakage current. The **Linear Integrated Systems** PAD series of diodes will exhibit immediate improvement in the circuits shown in the preceding figures. A 1N4148 has a typical reverse leakage of 25nA at 25°C with an applied reverse voltage of 20V. The PAD1 diode has a typical reverse leakage of 1pA at 25°C with an applied reverse voltage of 20V.

Similarly, the solution to junction capacitance problems can be addressed with the PAD series of diodes. Typical junction capacitance for a 1N4148 is 4pF. For the PAD1, typical junction capacitance is 0.5pF

Additional improvements in performance can be realized by adding a differential pair of junction FETs at the input of the op-amp. Shown in Figure 7, the JFETs are a matched pair in a single package, the **Linear Integrated Systems** LSK389.

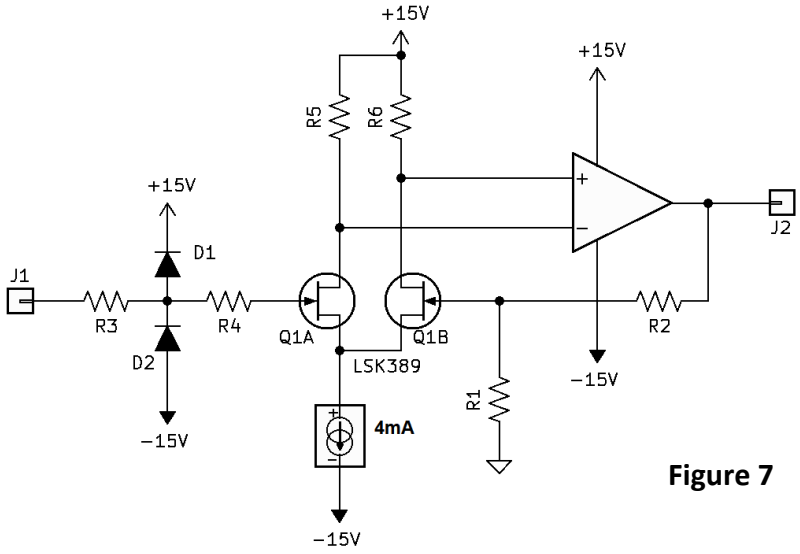

Figure 7

For a more detailed look at a real-world application, see Figure 8. This is a wideband amplifier having ±5000 VDC supply rails for the output stage. It is used in an electron energy separation device for an electron-beam machine. The output stage is unique. Where one might expect to see a complimentary pair of high-voltage transistors and suitable level shifting circuitry to drive them, instead there is a pair of specialty opto-couplers. The OC-100-HG devices are made by **Voltage Multipliers, Inc.** They consist of a pair of LEDs that illuminate photodiodes that have a reverse voltage rating of 10 kV. Current gain is about 0.01% (the ratio of LED forward current to diode photocurrent). This seems low, but as part of an amplifier comprised of an op-amp and discrete transistors, it is entirely acceptable. Overall, the closed loop gain is 60 dB.

The driving circuitry for the LEDs is a balanced 40 dB non-inverting differential current amplifier steered by a low offset voltage FET input op-amp (U1). The voltage swing at the output of the op-amp (and thus the drive current to the subsequent current mirror stages) is clamped to about ±5.7 V. The clamp circuitry is made up of the Zener diodes D6 and D8 plus the PAD1 pico-amp diodes D5 and D7. The Zener diodes are 5.1 V devices; the additional diode drop voltage produces the ±5.7 V clamp. Resistors R5 and R7 force sufficient current through D6 and D8 when clamping to produce a sharp knee in the characteristic Zener V-I curve. D5 and D7 isolate the clamp circuit from the op-amp's sensitive summing node when not clamping. The clamp limits the output stage drive current to the opto-coupler LEDs to about 1 A (peak) and the high-voltage output currents to less than 10 mA.

Matched **Linear Integrated Systems** dual bipolar transistors (LS312 and LS352) are used in the cascaded precision current mirror stages. These complimentary current mirrors allow a single potentiometer (R20) to adjust currents to both the upper and lower high voltage output stage.

Additional protection for the op-amp is provided by PAD1 diodes D3 and D4. As with D5 and D7 (above), these diodes present no discernable parasitic load and minimize interaction with the summing node during normal operating conditions. However, in the event of a high voltage arc, unpredictable voltages may appear at the summing node of the op-amp via the capacitive elements in the feedback network (C3 and C2).

Even with such low capacitance values, arcing transients have such rapid rise times that fairly high voltages would be present at the op-amp's summing node if D3 and D4 were not present.

One final note on this design: This circuit uses an extremely high value feedback resistor (R4, 1.0 GΩ). Compensation of a high voltage amplifier with 60 dB of gain with such a high value of feedback resistor is difficult. Instead of trying to tweak the overall high frequency characteristics of the amplifier with capacitors in the femto-farad range, a far more practical method is used. A ratioed capacitive reactance divider network made up of R2, C1, R3, C3, R24, and the much more practical adjustable trimmer capacitor C2 allows for easy compensation. See Reference 2 again for helpful information on working with extremely high value resistors.

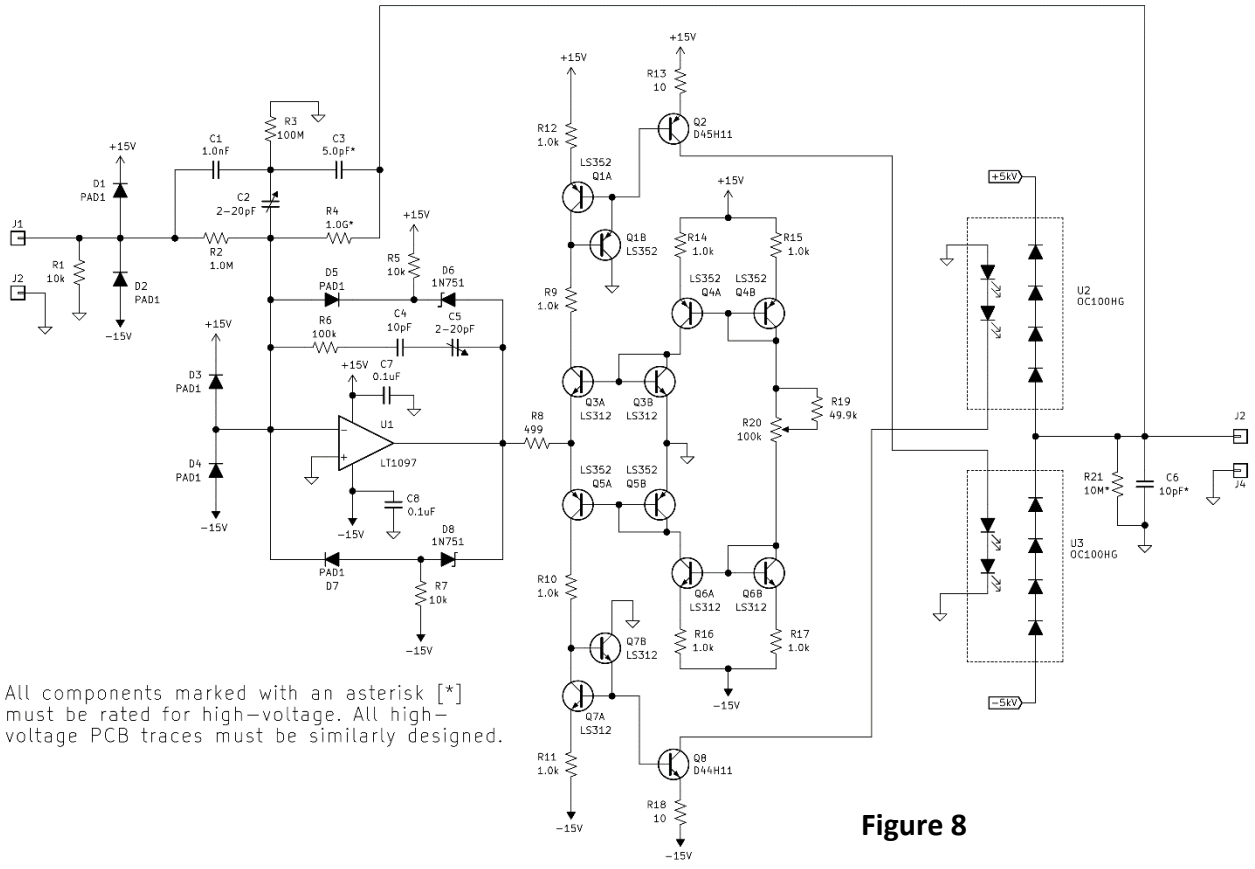

Figure 8

References:

1. Human Body Model (HBM) and Electro-Static Discharge (ESD):
Human-Body Model and Electrostatic Discharge (ESD) Tests

Comparison of Test Methods for Human Body Model (HBM) Electrostatic Discharge (ESD)

The ESD Association and JEDEC Publish New Revision to Standard for Electrostatic Discharge Sensitivity Testing

2. Design Femtoampere Circuits with Low Leakage, part 1, part 2